

STOC	nastic	Lom	DUTIN

SC data representation											
• Bernoulli Sequence as unipolar Bit Stream (BS).											
•	Value	equa	al to t	he r	ratio	o of	⁻ 1s	l			
•	Value	irrele	evant	to	ord	erc	of 0	s ar	nd 1	Ls	
•	 Value within (0, 1) 										
A=0.5	1 1 0	1	0 1	1	1	0	0	1	0	0	1
B_0.5			0 1	1	1	$\mathbf{\cap}$	4	$\mathbf{\cap}$	4		1
D=0.0						U		U		U	
C=0.75	1 0 1	1	0 1	1	1	1	1	0	1	0	1
 SC circuit and correlation SC multiplication with a single AND gate Extremely simple logic Ultra-low power Resistant to noise Level of paired 1s indicate SC correlation Varying correlation leads to function varying (from MIND) MUL 1010010010100 (6/16)											
$MIN \qquad \begin{array}{c} 1010010010100100 (6/16) \\ 1010010010110101 (8/16) \end{array} \qquad \begin{array}{c} \text{AND} \end{array} \qquad \begin{array}{c} 1010010010010010010010010010010001000000$											
Nonlinear functions in neural networks											
NN		Opera	ation								
CNN	Conv E		olina	R۵		•	Mc	ore	nor	nlin	ear

ININ	Operation		
CNN	Conv, FC, Pooling, ReLu	•	More nonlinea
LSTM	*, Div, Exp, Tanh		emerging NNs
Graph CNN	*, Div, Exp, Log, Sqrt	•	Stochastic com
CapsNet	*, Div, Exp, Log, Sqrt		better hardwar

Evaluating metrics

ISCBDIV performance

43.3% lower in error

New metrics to deal with feedback loops

Metric	Definition	0.25	
SCC	Stochastic Cross Correlation for 2 BSs.	0.2	GDIV
SAC	Stochastic Auto Correlation for 1 BS.	0.2 0 0 0 15	
WBS	N-Window Bias: accumulative error for the most recent N bits; ranging from -1 to 1; expecting 0 for no error.	178-4011 178-4011	_
AWBS	Average N -Window Bias: statistical root-mean-square of multiple N -WBS values.	0.05	16
<i>p</i> % CTime	p% Convergence Time: cycle count required for SCU to achieve a stable <i>N</i> -WBS of less than $p%$; smaller is better.	0	0-0.2

In-Stream Stochastic Division and Square Department of Electrical and Computer Engineering UNIVERSITY OF WISCONSIN-MADISON Di Wu and Joshua San Miguel



Evaluation and Implementation

46.3% faster in convergence







-Quotient

System reaches equilibrium: $P_{Dividend} = P_{Quotient} * P_{Divisor}$

System reaches equilibrium: $P_{In} = P_{Out} * P_{Out}$

BS inputs to CORDIV Kernel are positively correlated

 $P_{Quotient} = P_{Dividend} / P_{Divisor}$ $=\frac{\#(1)_{Dividend}}{}$ $\#(1)_{Divisor}$

+--Quotient

Feedback loops

introduce fluctuation in resulting BS, leading to output deviation.

BISQRT performance

• JKDIV-BISQRT reduces error by 16.8%. ISCBDIV-BISQRT reduces error by 29.0%.





Meeting correlation Hardware implementation requirements for different operators improves accuracy.

Module	Desired	
MUX	0	-
JKDIV	-	-
ISCBDIV	-	-

SC correlation tabl

Proposed SC DIV and SQRT

Random Bit ---- 2-bit Dividend -Skewed Synchronizer FSM Divisor JKDIV based BISQRT



Bit Inserting Square Root (BISQRT)





In-Stream Correlation Based Division (ISCBDIV)

Leveraging CORDIV Kernel with correlation



Skewed Synchronizer pairs up 1s for maximal correlation. 2-bit Shift Register

improves randomness.



Connecting port J to 1 leads to

$$P_Q = P_J / (P_J + P_K)$$

$$= \frac{1}{1 + P_K}$$

SC SQRT output is less than input. $\sqrt{0.81} = 0.9 > 0.81$ Insert 1s to input leads to correct SQRT in SC.

> Functionality is guaranteed if $P_{Trace} = 1/(1 + P_{Out})$

Simplified ISCBDIV

Output of CORDIV Kernel comes from the SR for isolation $P_{Quotient} = 0.5/(0.5 + 0.5 * P_{Out})$

$$h_{t} = 0.3/(0.3 \pm 0.3) *$$

= $\frac{1}{1}$

$$1 + P_{Out}$$

naruware implementation								
•	For DIV, energy reduction is 67.6%.							
•	For JKDIV/ISCBDIV SQRT, reduction							
	72.8%/47.8%	6 in e	nergy	/sqrt.				
	Desimu	Area	Power	Latency	TPA			

is

al	Design	Area	Power	Latency	TPA
	Design	(μm^2)	(μW)	(cycles)	$(1/(\mu m^2 \cdot s))$
	GDIV(Depth-5)	74.3	21.0	158	34,073
	CORDIV	211.2	60.9	226	8,384
	Proposed ISCBDIV	40.4	12.5	86	115,128
	GSQRT(Depth-5)	78.3	23.5	192	26,607
Ιο	Proposed JKDIV BISQRT	11.3	6.3	195	181,529
IE	Proposed ISCBDIV BISQRT	25.4	12.6	187	84,214